The Interaction of Compilation Technology and Computer Architecture

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The Interaction of Compilation Technology and Computer Architecture David J. Lilja, Peter L. Bird In brief summary, the following results were presented in this work: • A linear time approach was developed to find register requirements for any specified CS schedule or filled MRT. • An algorithm was developed for finding register requirements for any kernel that has a dependence graph that is acyclic and has no data reuse on machines with depth independent instruction templates. • We presented an efficient method of estimating register requirements as a function of pipeline depth. • We developed a technique for efficiently finding bounds on register require ments as a function of pipeline depth. • Presented experimental data to verify these new techniques. • discussed some interesting design points for register file size on a number of different architectures. REFERENCES [1] Robert P. Colwell, Robert P. Nix, John J O'Donnell, David B Papworth, and Paul K. Rodman. A VLIW Architecture for a Trace Scheduling Com piler. In Architectural Support for Programming Languages and Operating Systems, pages 180-192, 1982. [2] C. Eisenbeis, W. Jalby, and A. Lichnewsky. Compile-Time Optimization of Memory and Register Usage on the Cray-2. In Proceedings of the Second Workshop on Languages and Compilers, Urbana l/inois, August 1989. [3] C. Eisenbeis, William Jalby, and Alain Lichnewsky. Squeezing More CPU Performance Out of a Cray-2 by Vector Block Scheduling. In Proceedings of Supercomputing '88, pages 237-246, 1988. [4] Michael J. Flynn. Very High-Speed Computing Systems. Proceedings of the IEEE, 54:1901-1909, December 1966.

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